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Design Of Low Power Approximate Mirror Adder

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ABSTRACT: Addition is a fundamental operation for any digital system, digital signal processing and control system. A quick and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Low power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. In most of the multimedia applications human beings can gather useful information from slightly erroneous outputs. Therefore, we cannot need to produce exactly correct numerical outputs. Preceding research in this context exploits error resiliency primarily through voltage over scaling, make use of algorithmic and architectural techniques to mitigate the resulting errors. In this paper, we propose logic difficulty reduction at the transistor level as an alternative approach to take advantage of the relaxation of numerical accuracy. We demonstrate this idea by proposing various imprecise or approximate full adder cells with reduced complexity at the transistor level, and make use of them to design approximate multi-bit adders. In addition to the inherent decrease in switched capacitance, our techniques result in significantly smaller difficult paths, enabling voltage scaling. We design architectures for video and image compression algorithms using the proposed approximate arithmetic units and evaluate them to demonstrate the efficacy of our approach. We also derive clear mathematical models for error and power consumption of these approximate adders.

Index Terms: Approximate Mirror Adder, low power

1. INTRODUCTION

The adder is one of the most critical components of a processor, as it is profitable in the Arithmetic Logic Unit (ALU), in the floating-point unit and for address generation in case of cache or memory access. More demand for mobile electronic devices such as cellular phones and laptop computers requires the use of power efficient VLSI circuits. With exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI (very large-scale integration) systems have increased many folds. Wile rise in chip density, power consumption of VLSI systems is also increasing and this further, adds to reliability and packaging impact. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. Now a day's low power consumption along with minimum delay and area requirements is one of important

design consideration for IC designers.

Recent trends in micro-electronics technology have gradually changed the Strategies used in VLSI circuits. Establishing an efficient methodology is one of the key to design VLSI chip successfully. The design of microelectronics system is strongly influenced by the fact that transistor and featured size have continuously influenced, while density and frequency have increased .VLSI will undoubtly play a key role in a technical revolution which yields a great benefit through application in communications, leisure and education. The major advantages of VLSI technology might be as follows: development of new functions and application, low cost, light weight, and low power dissipation, improvement in reliability and safe, possibility of being used to highly sophisticated control system and more advanced service function through systemization.

Addition is a fundamental operation for any digital system, digital signal processing and control system. A quick and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also act as very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, to make Performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The action of a digital circuit block is gauged by analyzing its power dissipation, layout region and its operating speed.

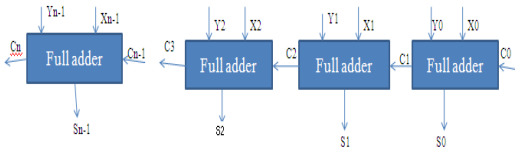


Fig.1 N-bit ripple carry adder.

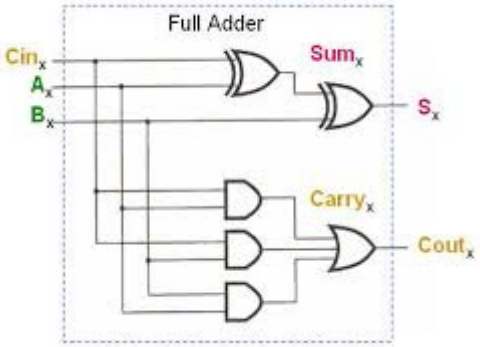


Fig .2 full adder (FA)

Ripple-Carry Adder (RCA): The n-bit adder built from n one-bit full adders is know as a ripple carry adder, because of the way the carry is computed. Each full adder inputs a Cin, which is the Cout of the preceding adder. This kind of adder is called a ripple carry adder, since each carry bit "ripples" to the next full adder. Block diagram of Ripple Carry Adder is as in Fig. 1.The layout of ripple carry adder is not so difficult, which allows for fast design time; however, the ripple carry adder is relatively not fast, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay cannot difficult be calculated by inspection of the full adder circuit. Each full adder requires A,B,Cin levels of logic. In a 32-bit (ripple carry) adder, there are 32 full adders, so the difficult path (worst case) delay is 31 * 2(for carry propagation) +3(for sum) = 65 gate delays.

11.APPROXIMATE ADDERS

In this section, we discuss different methodologies for designing approximate adders. We use RCAs and CSAs throughout our subsequent discussions in all sections of this paper. Since the Mirror Adder is one of the widely used economical implementations of an FA, we use it as our basis for proposing different approximations of an FA cell.

A. Approximation Strategies for the MA

In this section, we explain step-by-step procedures for coming up with various approximate Mirror adder cells with fewer transistors. Removal of some series connected transistors will facilitate faster charging/discharging of node capacitances. Moreover, complexity decrease by removal of transistors also aids in reducing the αC term (switched capacitance) in the dynamic power expression Pdynamic = αCV2DDf , where α is the switching activity or average number of switching
Transitions per unit time and C is the load capacitance being charged/discharged. This directly results in lower power dissipation. Area reduction is also achieved by this process. Now, let us discuss the conventional adder implementation followed by the proposed approximations.

*1)Conventional MA:*The Gate-level of a conventional adder, which is a popular way of implementing an FA.Since this implementation is not based on complementary cmos,it provides a good opportunity to design an approximate version with removal of selected transistors.

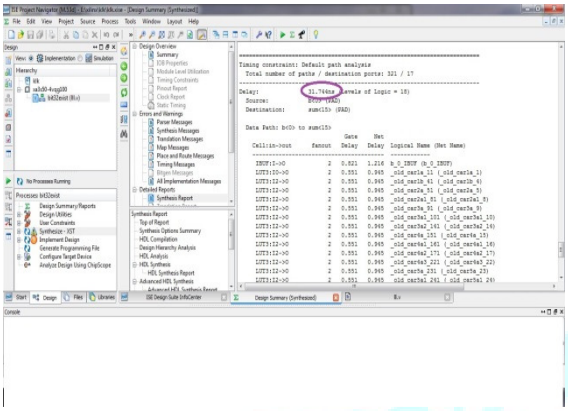
*2)Approximation 1:*In order to get an approximate Adder with fewer input gates, we start to remove c_{in} from the conventional adder one by one. However, we cannot do this in an arbitrary fashion. The input combination of *A, B* and *C*in does not result in short circuits or open circuits in the simplified schematic. Another important criterion is that the resulting simplification should introduce minimal errors in the FA truth table.

*3)Approximation 2:*In order to get an approximate Adder with fewer input gates, we start to remove input "B" form the conventional adder one by one. However, we cannot do this in an arbitrary fashion. The input A, B and *C*in does not result in short circuits or open circuits in the simplified schematic. Another important criterion is that the resulting simplification should introduce minimal errors in the FA truth table.

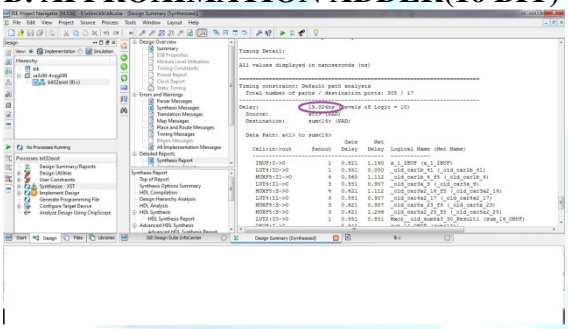
*4)Approximation 3:*In order to get an approximate Adder with fewer input gates, we start to remove input "A" from the conventional adder one by one. However, we cannot do this in an arbitrary fashion. The input *A, B* and *C*in does not result in short circuits or open circuits in the simplified schematic. Another important criterion is that the resulting simplification should introduce minimal errors in the FA truth table.
In above all these cases, there is one error in *C*out and four errors in Sum.

RESULT IN DELAY:

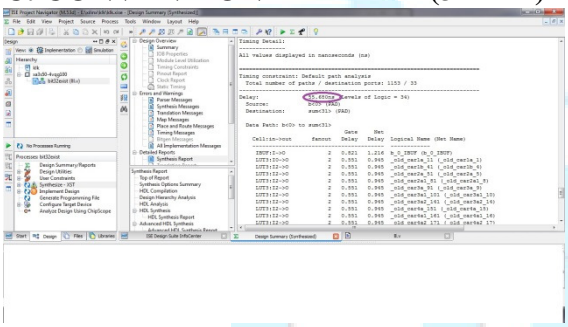
A. CONVENTIONAL ADDER(16 BIT)



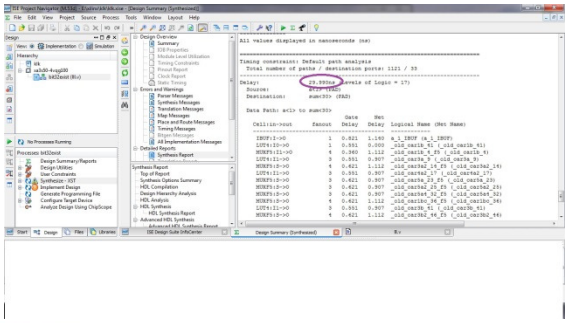
B. APPROXIMATION ADDER(16 BIT)



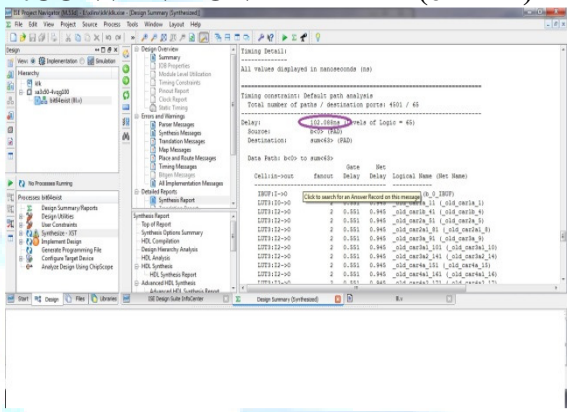
C. CONVENTIONAL ADDER(32 BIT)



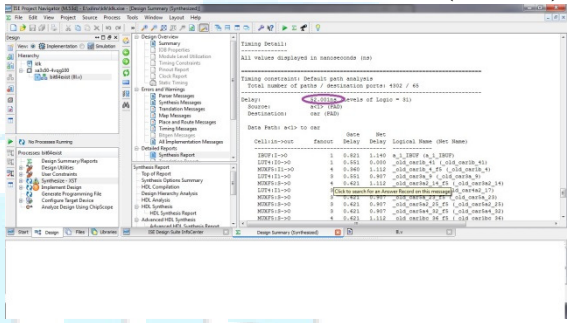
D. APPROXIMATION ADDER(32 BIT)



E.CONVENTIONAL ADDER(64 BIT)



F. APPROXIMATION ADDER(64 BIT)

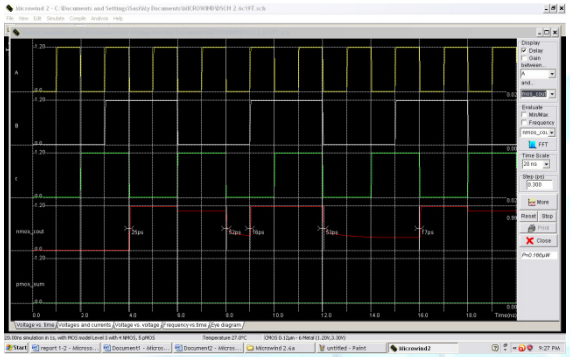


COMPARISON:

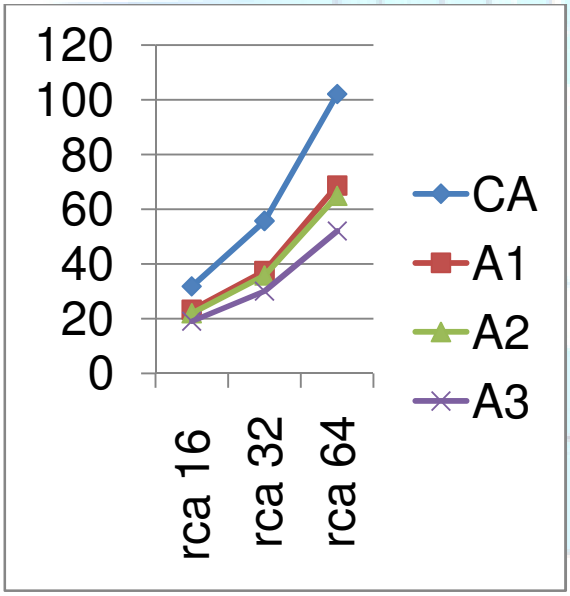
No. of bits	DELAY			
	Existing RCA (ns)	Proposed Output		
		A1	A2	A3
8	19.776	14.715	15.8	14.27
16	31.7	23.233	21.97	19.02
32	55.68	37.435	35.776	29.9
64	102	68.8	64.887	52

KEYWORDS:
A1- Approximation I
A2- Approximation II
A3- Approximation III

SIMULATION RESULT



PERFORMANCE ANALYSIS



111.CONCLUSION:

The 'APPROXIMATE ADDER' was thus designed with an idea to minimize the delay and power consumption The 'APPROXIMATE ADDER' was tested using the Xilinx ISE and was compared with the other conventional adders such as the Ripple carry adder. The power consumption of the 'Approximate adder' was calculated using the Micro wind/DSCH tool. Extensive comparisons with conventional digital adders showed that the proposed 'APPROXIMATE ADDER' outperformed the conventional adders in both power consumption and speed performance. The potential applications of the 'APPROXIMATE ADDER' fall mainly in areas where there is no strict requirement on accuracy or where super low power consumption and high-speed performance are more important than accuracy. In future we can implement the approximation technique in CARRY LOOK AHEAD ADDER(CLA) and it can be used in the DSP application for portable devices such as cell phones, laptops and medical imaging.

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